REMARKS/ARGUMENTS

This application has been carefully considered in connection with the Examiner's Action. Reconsideration and allowance are respectfully requested in view of the following.

A. Summary of the Amendment

Claims 1, 5, 9 and 22 have been amended and Claims 3-4, 15-16 and 25 have been canceled without prejudice or disclaimer. Accordingly, Claims 1-2, 5-14, 17-24 and 26-30 are pending before the Examiner.

B. The Objection to the Drawings

The drawings stand objected to as lacking descriptive labels on Figure 2 thereof. In response, the Applicants have prepared and submit herewith a *Request for Approval of Proposed Drawing Correction* for consideration by the Examiner. It is submitted that Replacement Drawings incorporating all of the proposed corrections set forth therein will remove all basis for the Examiner's objection to the drawings. Accordingly, the Applicants respectfully request approval of the proposed correction to Figure 2 and withdrawal of the objection to the drawings. Upon approval of the proposed drawing correction and an indication that the application contains allowable subject matter, the Applicants will submit Replacement Drawings which fully incorporate all drawing corrections approved by the Examiner.

C. The Rejection of Claims 3, 4, 15, 16 and 25

Claims 3, 4, 15, 16 and 25 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. While the Applicants respectfully disagree that usage of

relative terms such as those set forth in the referenced claims would render such claims indefinite, it is submitted that Applicant's cancellation of Claims 3, 4, 15, 16 and 25 have rendered the Examiner's rejection under the second paragraph of Section 112 as moot. Accordingly, the Applicants respectfully request the withdrawal of the rejection of Claims 3, 4, 15, 16 and 25 under 35 U.S.C. § 112, second paragraph.

D. The Rejection of Claims 1, 2, 5-14, 16-24 and 26-30

Claims 1, 2, 5-14, 16-24 and 26-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,835,429 to Schwarz (hereafter referred to as "Schwarz I") in view of U.S. Patent No. 6,496,947 to Schwarz (hereafter referred to as "Schwarz II"). In response, the Applicants respectfully traverse the Examiner's rejection and instead submit that Claims 1-2, 5-14, 17-24 and 26-30, as above amended, are neither taught nor suggested by the cited art. Accordingly the Applicants respectfully request the reconsideration and withdrawal of the rejection of Claims 1, 2, 5-14, 16-24 and 26-30 as unpatentable over Schwarz I in view of Schwarz II and the allowance of Claims 1-2, 5-14, 17-24 and 26-30, as above amended.

In rejecting the claims as unpatentable over Schwarz I in view of Schwarz II, the Examiner acknowledged that Schwarz I fails to disclose that "data is written into segments and then paused and then read." Examiner's Action dated February 24, 2006, page 4, lines 18-19. Characterizing Schwarz II as teaching an integrating circuit having "a built-in self repair (PISR) circuit which executes a sequence of read and write operations on a memory array and a pause circuit which pauses the sequence of write and read operation[s] for a pause time period," the Examiner rejected Applicants' claimed method and system of testing data retention of memory as unpatentable over the combination of Schwarz I and Schwarz II.

In response, the Applicants respectfully note that Schwarz II merely discloses a method of testing a memory array in which a built-in self test (BIST) circuit 18 activates pause circuit 20 to introduce a short pause in the test algorithm. As specifically set forth therein, "[t]his pause ensures that there is a predetermined delay between accesses in subsequent runs through the memory array." Schwarz II, col. 8, lines 15-17 (emphasis added by Applicants). In contrast with Schwarz II, Applicants' invention recognizes that, depending on the time period required to write data to the memory array being tested for data retention, it may or may not be necessary to insert a pause between the write and subsequent read operations. For example, if a relatively small memory array is being tested, a pause is required for the test to yield useful results. Conversely, however, when testing a large memory array, no such pause is required in order to determine whether the tested memory has a suitable data retention characteristic.

Accordingly, as amended herein, Applicants' invention is directed to a system and associated method of testing data retention of a memory which pauses between write and read operations only if the total time to required to write data is insufficient to determine the data retention capabilities of the memory. As such a feature is neither taught nor suggested by the operation of the pause circuit disclosed in Schwarz II, the Applicants respectfully submit that Claims 1-2, 5-14, 17-24 and 26-30, as above amended, are distinguishable over the art of record.

E. Concluding Remarks

For all the above reasons, the Applicants respectfully request the reconsideration and withdrawal of the objection to the drawings and various rejections of Claims 1-30 and the allowance of Claims 1-2, 5-14, 17-24 and 26-30.

This application is now considered to be in condition for allowance. A prompt Notice to that effect is, therefore, earnestly solicited.

No fees are believed to be required. If, however, any fees are deemed necessary, please charge these fees to LSI Logic Corporation, Deposit Account No. 12-2252. No extension of time is believed to be necessary. If, however, an extension of time is believed to be required, please charge any fees for this extension to LSI Logic Corporation, Deposit Account No. 12-2252.

Respectfully submitted,

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